FAMU/FSU College of Engineering

Department of Electrical and Computer Engineering

Scholarship in Practice

Team #302 – Design/Prototype a Multi-Platform Broadband Communication Payload for a Search and Rescue Operation

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Introduction

The aim of this document is to analyze major decisions the team made throughout the design process. A summary of the decisions is given and why they were made. An analysis of the decisions is performed, and better options are discussed. The team has learned a lot from the decision process and the lessons learned will be put into each members tool box for future projects.

Evaluation of Decisions

1. Power Source

The battery that the group initially desired was a rechargeable lithium-ion battery. However, when it came time to make the selection, a rechargeable lithium-ion battery pack within the weight requirements of the design could not be found. To estimate the overall power consumption of the FPGA and overall power provided by the battery, the group used equations for power such as those provided in Circuits 2 and Electronics.

This decision can be deemed suboptimal because although the battery pack that was selected does indeed power our design, they are not reusable, meaning more will have to be acquired after consumption. In a field such as search and rescue, this could be improved upon. Even with this flaw however, this decision provided useful experience on how best to go about estimating power consumption for devices such as FPGAs and other assorted boards.

2. Payload Housing

The payload housing was designed on paper using material strength and design equations taken from classes such as engineering mechanics. The housing was originally planned to be printed in one piece, however, this was unfeasible, so it will be printed in three separate pieces and assembled. This experience will prove valuable to us as electrical and computer engineers, as it gives relatively rare 3-D printing experience that is not found in many of our required courses.

Due to lack of knowledge with 3-D modeling design this was a weak-spot of the project design. If this was done again there are multiple different options that can be done. Since the team chose to do 3-D printing for the housing, more time should have been allocated to learn how to create 3-D models. If the time cannot be allocated to learn how to create 3-D models, then exploring out-sourcing options should be done. Since the material was light and the housing design was not intricate it would have been inexpensive to buy pre-made housing and edit it if needed.

3. FPGA

The FPGA is a crucial component to the overall project, so the team researched the chosen FPGA extensively. All members of the team used experience and information learned from digital logic design and microprocessors. This knowledge was used to assist in choosing and implementing the board in the design. Ultimately the decision on the FPGA was heavily weighed by the sponsor using the chosen board (Xilinx ZCU102) in their project that is parallel to the team's project. Due to shipping constraints the Xilinx ZCU102 board came in later than desired, leaving 2 months to work with the board.

Using knowledge developed from digital logic design and microprocessors the team believed it would be straightforward to learn how to use Vivado (software for Xilinx) and interfacing with other devices connected to the FPGA. To start learning Vivado and how to load VHDL projects onto the board a test design that was inspired by introduction to VHDL was used. Where a simple switch on the board would light up an LED based on its up/down state. Creating a simple design to become familiar with Vivado and loading a bit-stream (VHDL project) onto the ZCU102 board was extremely helpful. A modular based design was chosen as the way to implement the VHDL project. Where multiple sub VHDL projects would be used and instantiated in a top level design. These sub-modules consisted of interfacing with the transceiver, a sub-module for timestamping, one for timestamping and one for interfacing with Northrop Grummans' proprietary code. This modular based design approach was crucial to past course projects like digital logic design projects and so it was decided to do the same for this project.

The team realized while working on the VHDL project for the transceiver that the chosen board was more complicated to work with than expected. Interfacing with the transceiver and PMOD was originally believed to be done by using pinouts. After getting the data, analysis would be done, and results would be pumped to the SD card. This plan was too rudimentary. In the future a more detailed plan of how the VHDL sub-module designs work is required. With only two months to work with the FPGA the team did not have enough time to create successful sub-module VHDL projects. This was due to a lack of knowledge of how the board specifically works, where data was stored and sent to. In the future or if this design is done again a test or evaluation board should be used. A lot of time was lost during the design phase due to not being able to test and directly see results. The ZCU102 board also has a lot of components and features that took a lot of time to learn. Due to the time of the project a simpler board should've been used or extensive research on the components on the board should have been done before receiving the board.

4. Interfacing of Transceiver

As discussed in the previous section, the original plan for the FPGA involved using simple pin-out procedures like in Microprocessors or Digital Logic Design. The transceiver was decided based on knowledge from the Digital Communications course. At front the chosen transceiver met all the requirements needed for the design. Including frequency range, low noise amplifier, ADC, DAC, and other specs. The transceiver, however, did not come with detailed pin locations in the data sheet, so different methods had to be used. Due to the transceiver not having the pinouts in its data sheet this majorly hindered the design progress.

The data sheet of the transceiver not containing its pinout information was a major oversight of the team. In the future when buying/choosing parts checking to ensure the part you are implementing can be implemented in the desired way no matter how simple the method. Data sheets containing pinout information was assumed, since all parts in past work always contained it. This was a mistake and should not be assumed in the future.

However, it did provide valuable information on the real-world operation of an FPGA and how best to assign pins to operate on them, which will be vital information on any project that requires them to go forward.

5. Testing of Design

The design was tested by attaching an antenna to a signal generator in the senior design lab, projecting a signal and seeing if that signal can be detected by the oscilloscope software in the Linux environment booted off the FPGA. Signals in the range of 40MHz to 1GHz were tested. The design was tested at extended range projecting a signal from the senior design lab and placing the design on the first floor. This proved to be suboptimal as there is a lot of electrical noise in the College of Engineering and there are many concrete walls to attenuate the signal.

Testing of the design should have been considered more during part selection. Not coming up with a test process during the part selection hindered how the team could test the design later. Due to not ordering additional parts that could have been used to test the design the team was limited to what was in the lab. The limitation is mainly the team using a "weak" signal generator. The lab's signal generator was not strong enough to test the range at which the communication payload could pick up. Testing of the design was overall successful, but in the future in depth ideas of how to test should be done at the beginning of the design phase.

6. Part Selection

Parts were selected using houses of quality and Pugh charts, as was taught in engineering design concepts. In the future, less theoretical methods of selection could be used, and hard data could be used instead, with more research being done on the interfacing of the parts, beyond checking for compatibility of connectors.

This decision proved valuable as it will of course aid us in further part selection, which is almost certain to be a part of any future project.

7. Disbursement of Work

Due to the board license being limited to one device, this created a bottleneck in terms of how much manpower could be actively used in development. Instead of having all four members of the team working on different pieces of the design (such as the transceiver, the VHDL and the FPGA communication protocols), what ended up happening was two members worked on the bulk of the coding. This, paired with unforeseen issues with the provided Linux environment, severely hampered efforts to advance the project in a timely manner.

8. Linux Environment

The Linux environment was used as it was provided by the manufacturer of the transceiver, Analog Devices (AD). We learned how to use a Linux environment for embedded systems applications, such as in Intro to Unix Tools. This choice proved to be suboptimal as it required more human control of the system than desired. A better solution would have involved modifying the provided HDL project from AD to automate the human control in the current design.

Conclusion

In conclusion, although there were several things that could be improved upon in the overall design, such as battery selection and housing construction, the design process provided a vast amount of practical experience and taught numerous real-world applications of information from classes. Some of these applications being the use of power analysis from Circuits 2, physical design calculations from Engineering Mechanics, FPGA interfacing from Microprocessors, and Linux operation from Intro to Unix tools, along with many other skills from various classes. Therefore, despite whatever the outcome of the project was, it can be assumed to be a success, as it provided an immense amount of real-world experience in engineering projects and gave a real glimpse into operating under pressure such as deadlines, budgets, and provided design constraints.